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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,615	01/27/2004	Shiv Kumar Gupta	15397US01	1349

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,615	GUPTA ET AL.	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 7, and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 3, 7, and 11 recites the limitation "the selection" in lines 3 and 4, line 4, and line 4 for the respective claims. There is insufficient antecedent basis for this limitation in the claim. Claims 3, 7, and 11 all cite "a selection" with regards to a data multiplexer, while the preceding claims they are respectively dependent from (Claims 2, 6, and 10) cite "a selection" with regards to an address multiplexer.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Rana, U.S. Patent 5,968,188.

6. Referring to claim 1, Rana teaches a emulation circuit, which provides real-time code coverage data, connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a circuit for analyzing code coverage of firmware by test inputs, said circuit comprising: an input for receiving an address from a code address bus (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory, this is interpreted as a memory for storing recorded addresses form the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana also teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff", this is interpreted as the contents of the memory location associated with the address received from the code address bus being incremented responsive to the receipt of the address (See Col. 8, lines 31-44).

7. Referring to claim 2, Rana discloses the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, this is interpreted as an address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory (See Col. 4, line 65 to Col. 5, line 3 and Col. 5, lines 11-18).

8. Referring to claim 3, Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff", this is interpreted as a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory (See Col. 8, lines 31-44).

9. Referring to claim 4, Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" to locations accessed for each test, this is interpreted as wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address from the address counter is cleared (See Col. 8, lines 31-44).

10. Referring to claim 5, Rana teaches a method of real-time code coverage with a emulation circuit connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a method for analyzing code

coverage, said method comprising: receiving an address form a code address bus, the address associated with an instruction in a system on a chip (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18). Rana also teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff", this is interpreted as incrementing a memory location mapped to the address associated with the instruction (See Col. 8, lines 31-44).

11. Referring to claim 6, Rana discloses the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, this is interpreted as selecting between the input and an address counter; and providing the selection to the memory (See Col. 4, line 65 to Col. 5, line 3 and Col. 5, lines 11-18).

12. Referring to claim 7, Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff", this is interpreted as selecting between an increment signal and a clear signal; and providing the selection to the memory (See Col. 8, lines 31-44).

13. Referring to claim 8, Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" to locations accessed for each test, this is interpreted as wherein if the clear signal is selected, and if the address counter is selected, then clearing a memory location mapped to an address from the address counter (See Col. 8, lines 31-44).

14. Referring to claim 9, Rana teaches a emulation circuit, which provides real-time code coverage data, connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a circuit for analyzing code coverage of firmware by test inputs, said circuit comprising: an input for receiving an address from a code address bus (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory, this is interpreted as a memory operably connected to the input for storing recorded addresses form the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana also teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff", this is interpreted as the contents of the memory location associated with the

address received from the code address bus being incremented responsive to the receipt of the address (See Col. 8, lines 31-44).

15. Referring to claim 10, Rana discloses the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, this is interpreted as an address multiplexer connected to the input and address counter, the address multiplexer making a selection between the input and an address counter, and for providing the selection to the memory (See Col. 4, line 65 to Col. 5, line 3 and Col. 5, lines 11-18).

16. Referring to claim 11, Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff", this is interpreted as a data multiplexer connected to the memory, the data multiplexer selecting between an increment signal and a clear signal, and providing the selection to the memory (See Col. 8, lines 31-44).

17. Referring to claim 12, Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to "00" and changing it to value "ff" to locations accessed for each test, this is interpreted as wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address from the address counter is cleared (See Col. 8, lines 31-44).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are closely related code coverage systems.

U.S. Patent 6,708,143 to Kurshan

U.S. Patent App. Pub. 2005/0193254 to Yee

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
December 10, 2006